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HSF Property: ROHS

ACER_BAP31U

MAIN BOARD

2009.05.13

Wednesday, May 20, 2009		A01
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE	INVENTEC			
DRAWER					TITLE ACER_BAP31U			
DESIGN								
CHECK								
RESPONSIBLE								
SIZE:					I VER:			
FILE NAME: XXXXXXXXXXX-XX					SIZE	CODE	DOC NUMBER	REV
P/N	XXXXXXXXXXXX				C	AX1	D-CS-1310A2264501-ALG	A01
					SHEET		1 of 35	

1. Schematic Page Description :

Montevina Schematic Ver : A02

1. Title

2. Schematic Page DESCR

3. Block Diagram

4. Annotations

5. Schematic Modify

6. Timing Diagram

7. Power Block Diagram

8. Adaptor in/Charge

9. 5VLA/5VA/3VA

10. 3VS/5VS/1.5V (DDR3)

11. 1.05VS/1.5S/1.8V/1.5VA

12. Power Latch/1.5VS/SCREW HOLE

13. CPU Core Power

14. GPU Core Power

15. Penryn Processor(1/2)

16. Penryn Processor(2/2)

17. CPU Thermal
18. Cantiga Host(1/6)

19. Cantiga DMI/Graph(2/6)

20. Cantiga DDRII(3/6)

21. Cantiga Power(4/6)

22. Cantiga Power(5/6)

23. Cantiga Ground(6/6)

24. Clock Generator

25. DDR3 SDRAM SO-DIMM0

26. DDR3 SDRAM SO-DIMM1

27. ICH9M CPU/IDE/SATA(1/4)

28. ICH9M PCI/PCIE/DMI/USB(2/4)

29. ICH9M GPIO(3/4)

30. ICH9M Power/GND(4/4)

31. LCD CNN/SATA/3G/WLAN

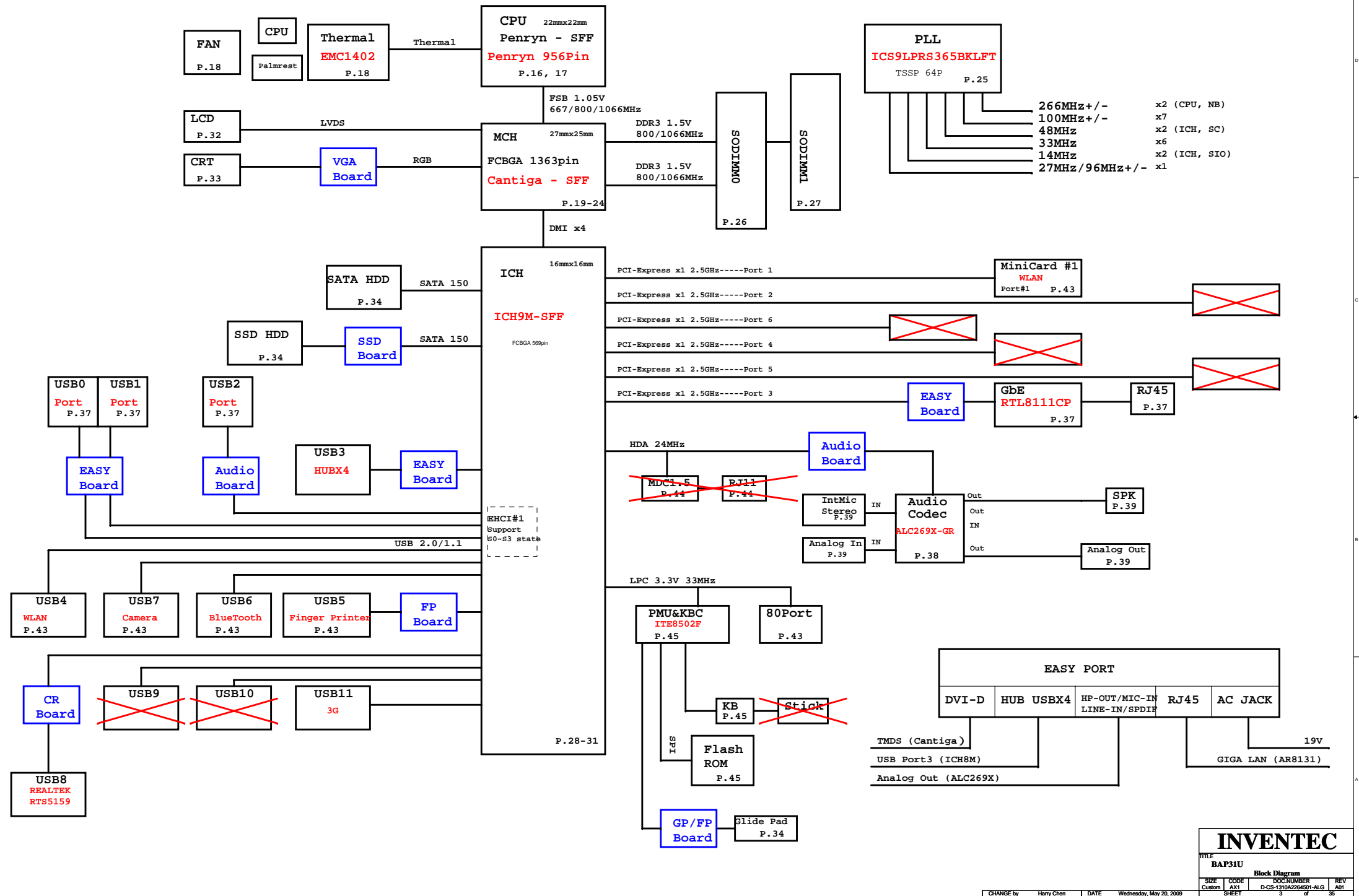
32. KBC ITE8512F

33. IO CN

34. IO CN

35. AUDIO CODEC

3. Block Diagram :



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

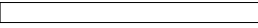



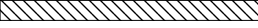


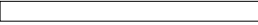
C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal
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5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM: LFM:	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	18A
1.05VS	Penryn SFF : AGTL+ termination Cantiga GS: Core Cantiga GS: PCIE Cantiga GS:Core+IMEL+HSIO Cantiga GS:VCC_GMCH Cantiga GS:VCCA_SM_CK and NCTF Cantiga GS:VCC_DMI Cantiga GS:VCCA_SM Cantiga GS:VTT ICH9M:VCC1_05 ICH9M:DMI ICH9M:CPU_IO	1V-1.05V-1.10V 0.997V-1.05V-1.102V 0.9975V-1.05V-1.1025V 0.9975V-1.05V-1.1025V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V	4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA
1.5VS	Penryn SFF PLL Cantiga GS: QDAC Cantiga GS: LVDS Cantiga GS: TVDAC Cantiga GS: Various PLLS analog supply Cantiga GS: VCC_SM_CK Cantiga GS: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card:	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.71V-1.8V-1.89V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA 650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V-1.5V-1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII:DDRIII Terminator:	0.7125V-0.75V-0.7875V	1.0A
3VS	Cantiga GS: HV CMOS Cantiga GS: VCCS_TVDAC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9PLRS365BKLFT Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC:	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA
1.8VS	DVI	3.0V-3.3V-3.6V	120mA
3VA	ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:AR8131 Azalia MDC: Flash ROM: BIOS	2V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	6uA 212mA 73mA 78mA 2A 1A
5VS	Cardreader: RTS5159 Azalia Codec: ALC269 HDD: SATA ODD: SATA Audio AMP: G1432 Inverter: WebCam	3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
5VA	USB: x 2 ports USB	5VA 5VA	1A 2A 1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V-3.3V-3.6V	300mA

INVENTEC

TITLE
BAP31U

ANNOTATIONS

SIZE
Custom

CODE
AX1

DOC NUMBER
D-CS-1310A2284501-ALG

REV
A01

CHANGE by Harry Chen DATE Wednesday, May 20, 2009

SIZE
CUSTOM

4

35

6.Schematic modify Item and History :

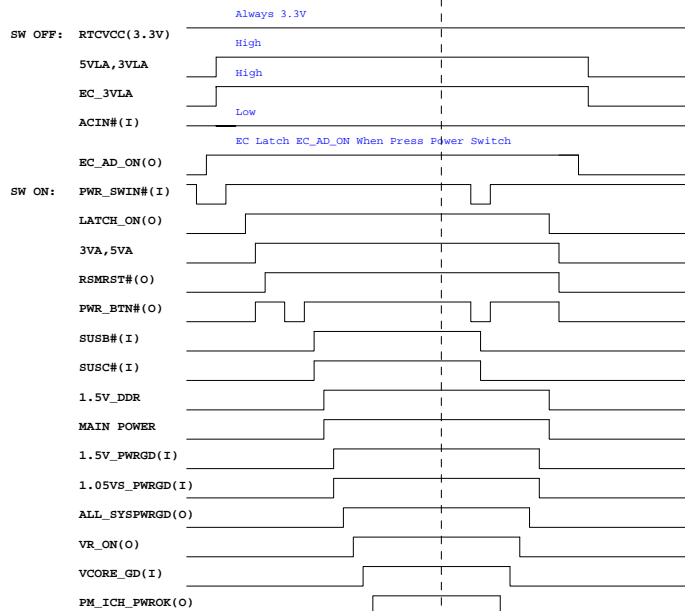
INVENTEC			
TITLE BAP31U			
Schematic Modify			
SIZE Custom	CODE AX1	DOC NUMBER D-CS-1310A2284501-ALG	REV A01

SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

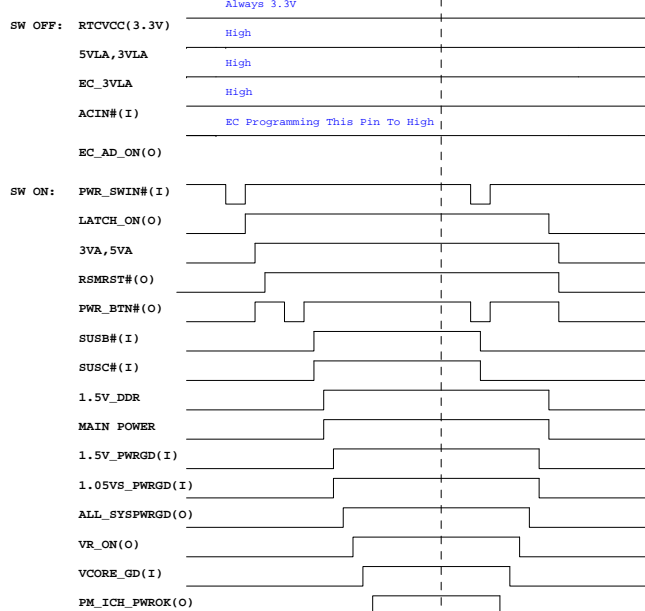
Power on/off sequence AC insert (without Battery Pack)

Power on sequence Power off sequence



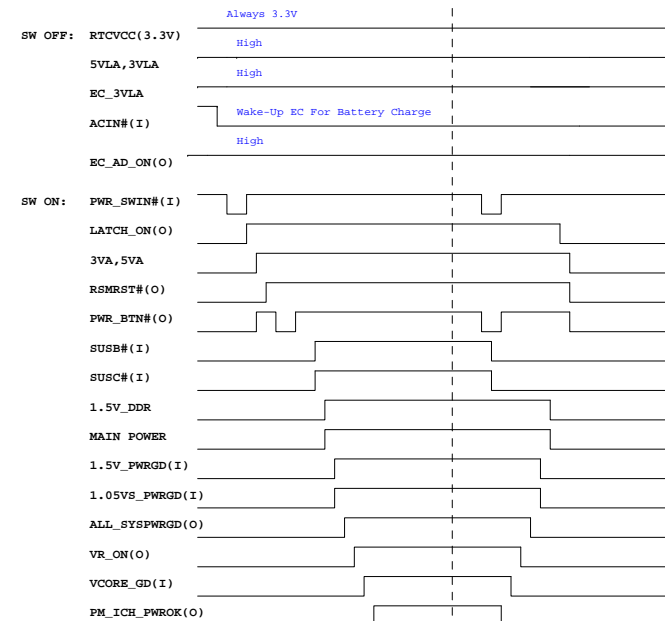
Power on/off sequence Battery insert (without AC adapter)

Power on sequence Power off sequence



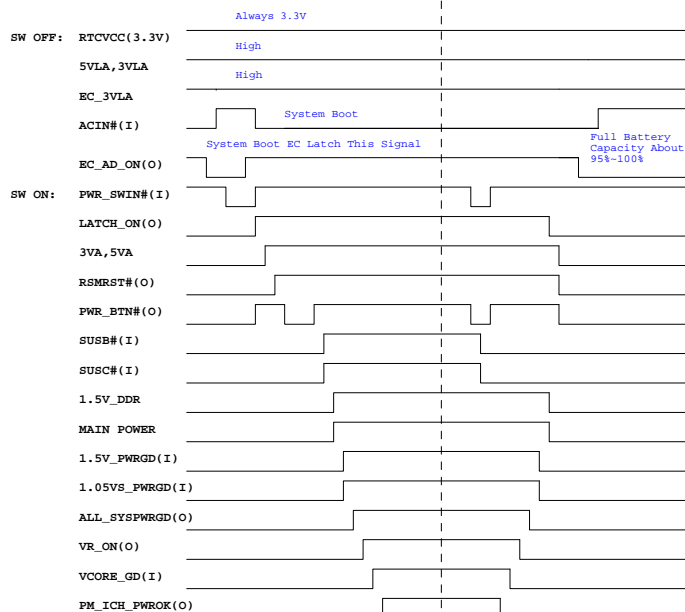
Power on/off sequence AC insert(with charge over 95%)

Power on sequence Power off sequence



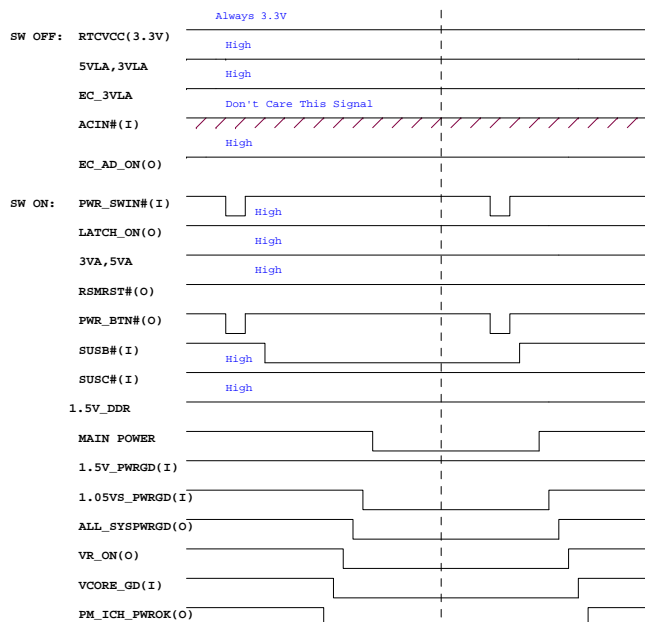
Power on/off sequence AC insert(without charge over 95%)

Power on sequence Power off sequence



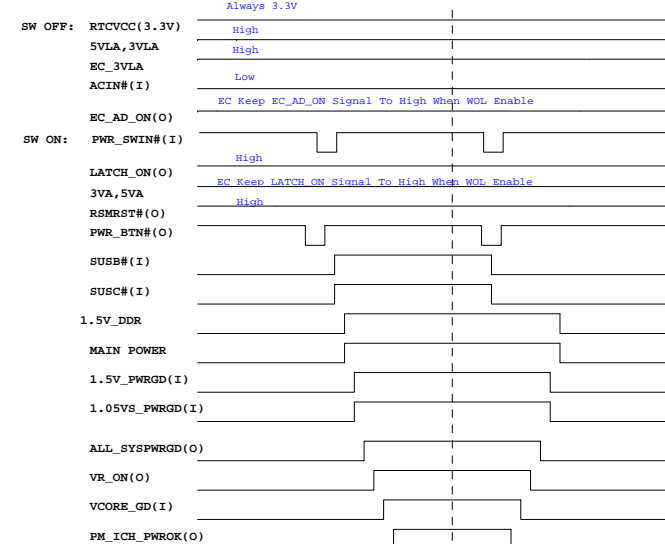
Suspend And Resume Sequence (S3)

Suspend sequence Resume sequence



Power on/off sequence after windows shoutdown (WOL enable)

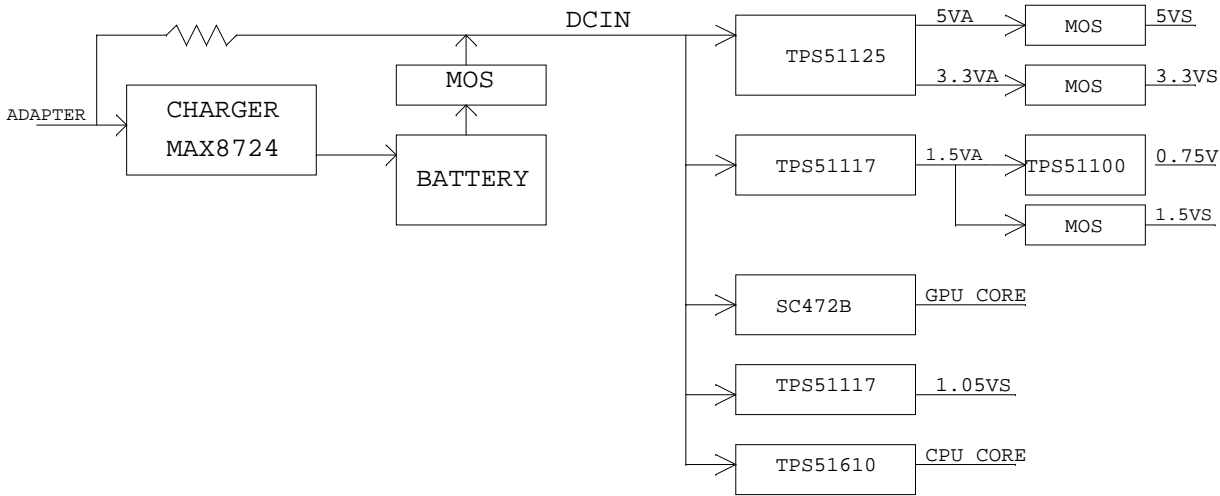
Suspend sequence Resume sequence

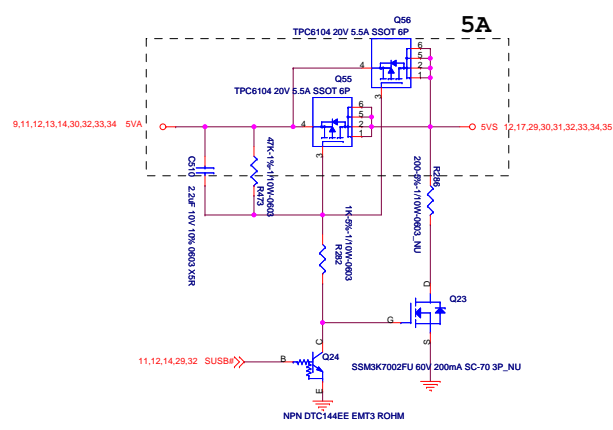
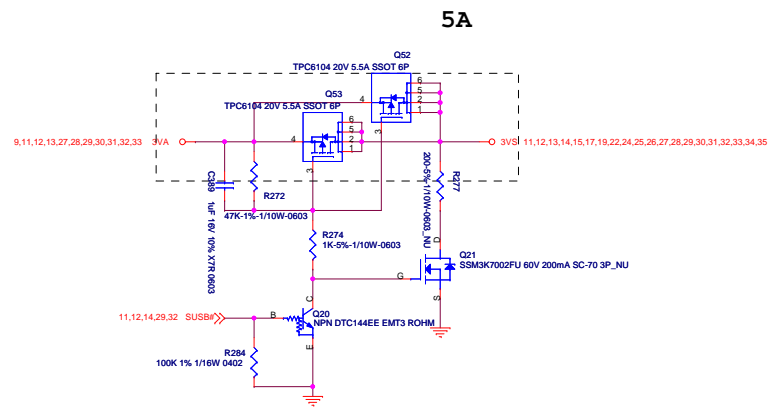
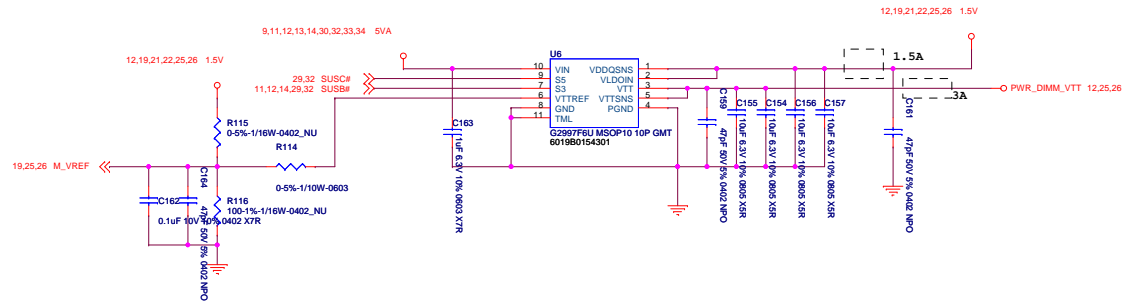
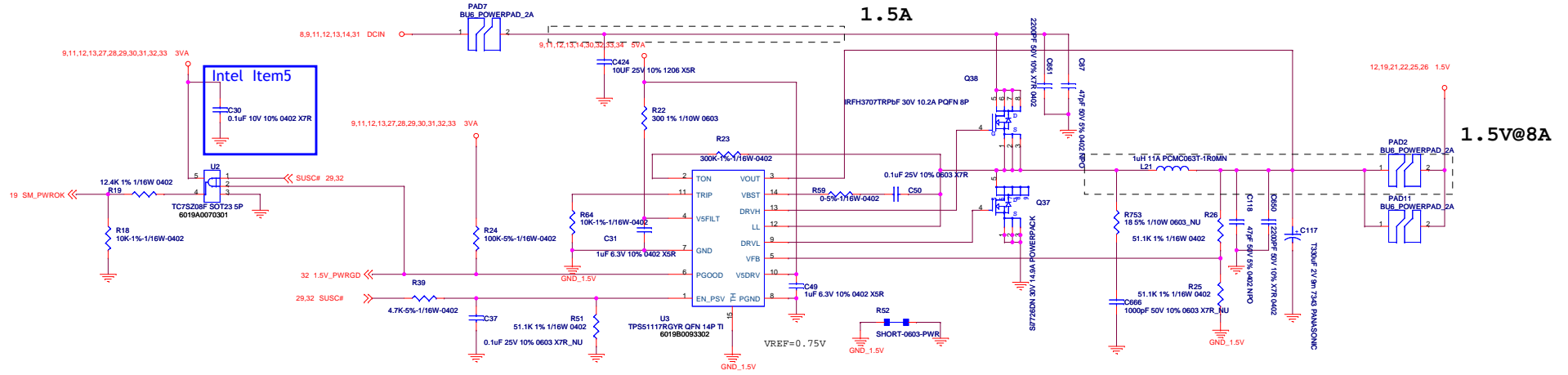


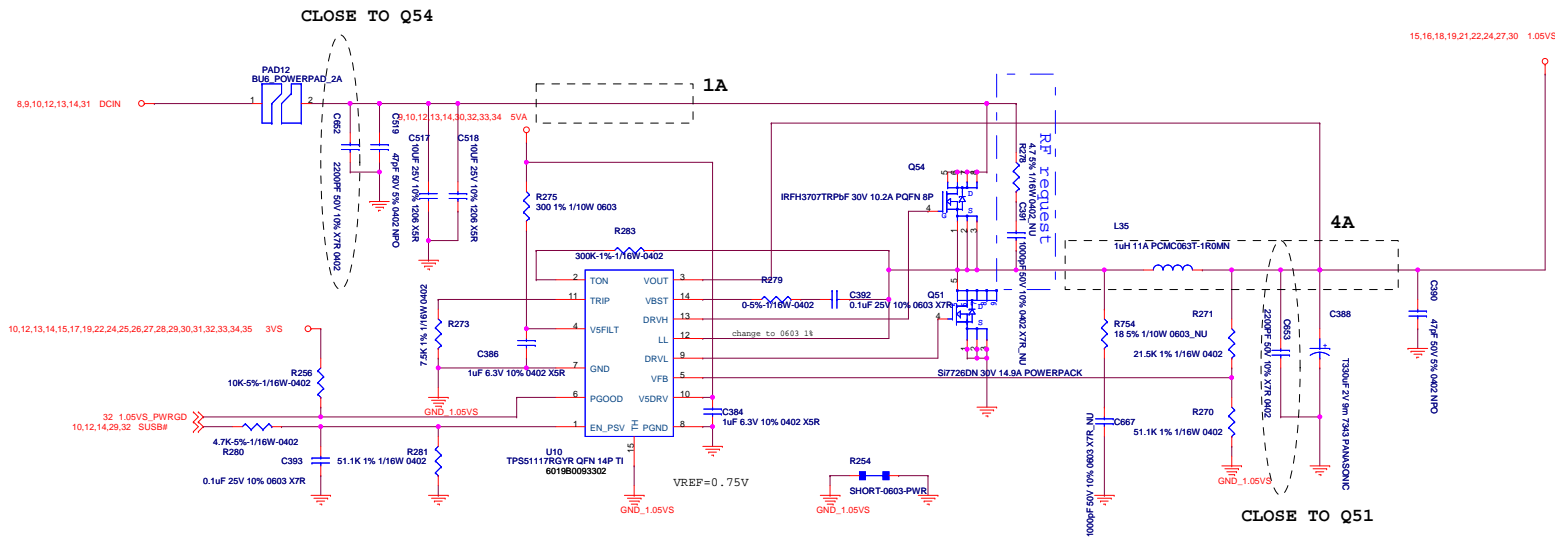
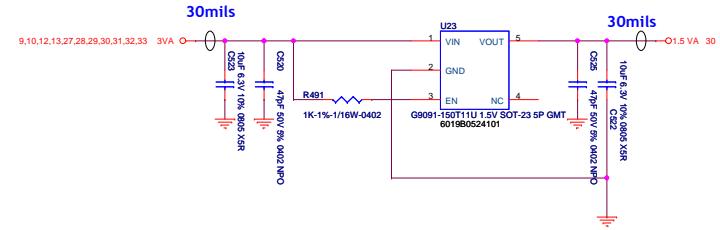
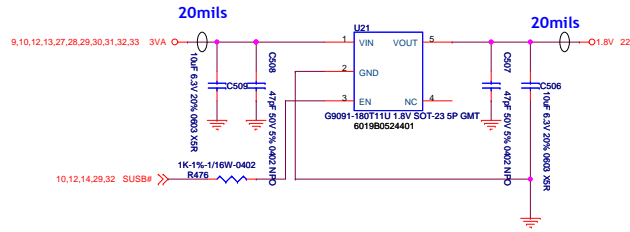
INVENTEC

TITLE		BAP31U		Time Diagram	
SIZE	CODE	DOC NUMBER	REV		
Custom	AX1	D-CS-1310A264501-ALG	A01		
SHEET		6	of	36	

Power Block Diagram :

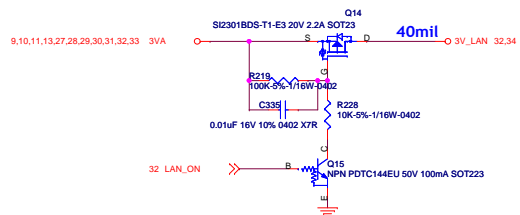
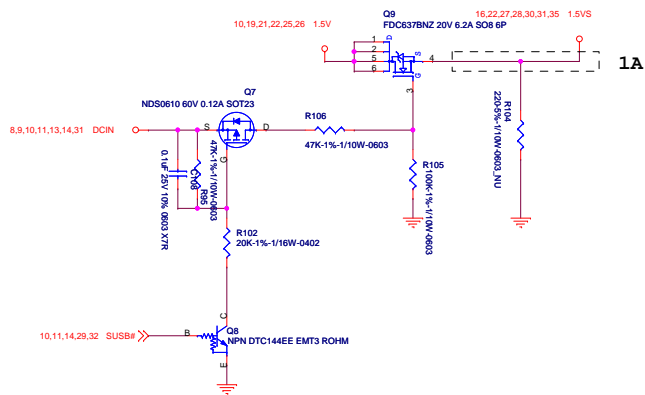




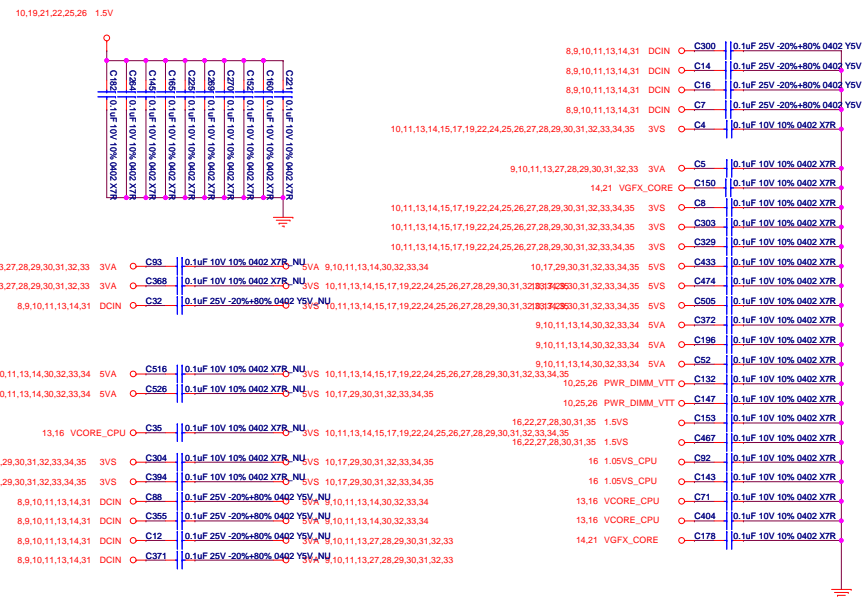


INVENTEC			
TITLE BAP31U			
1.05VS/1.5S/1.8V/1.5VA			
SIZE Custom	CODE AX1	DOC NUMBER D-C8-1310A2264501-ALG	REV A01
SHEET		11	of 35

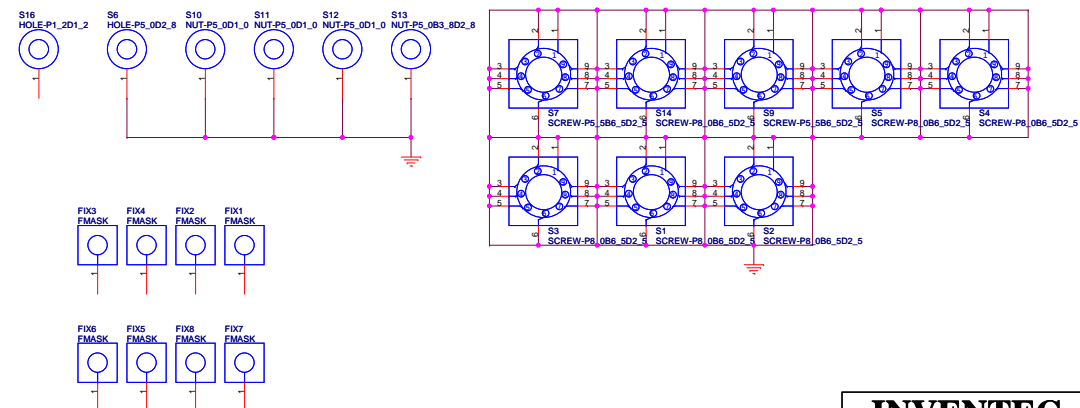
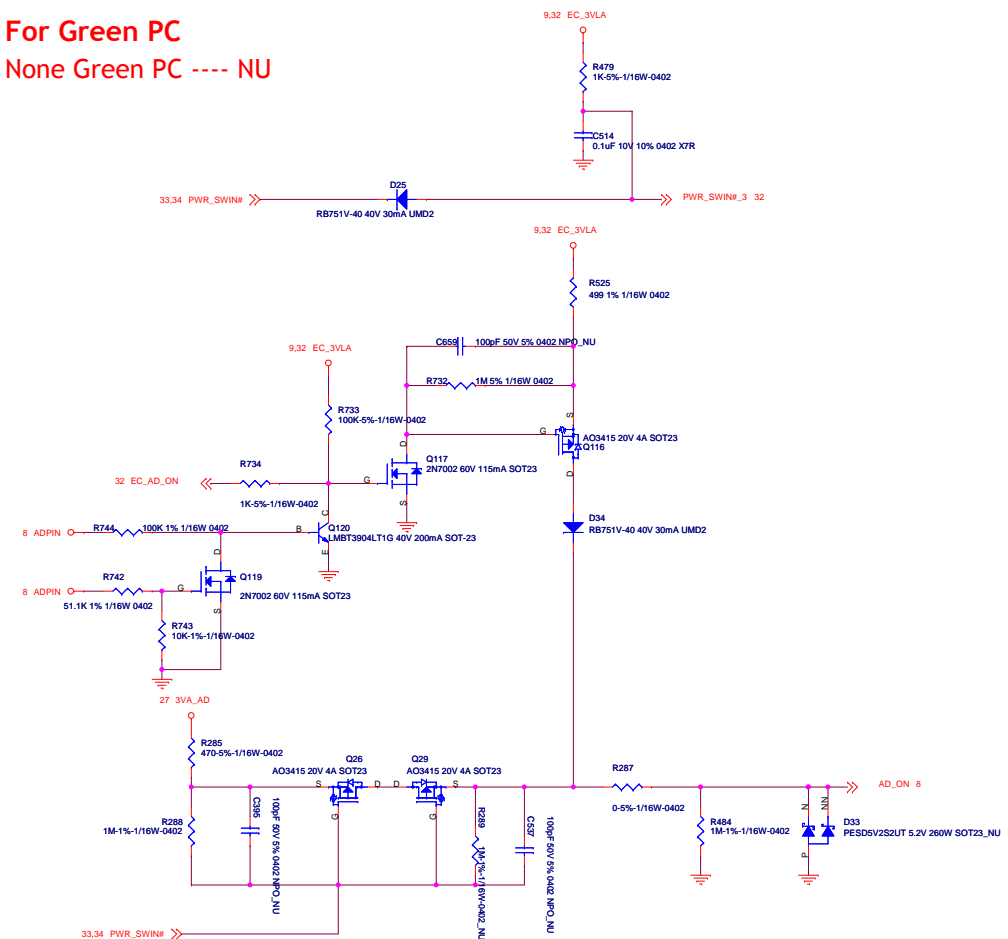
1.5VS

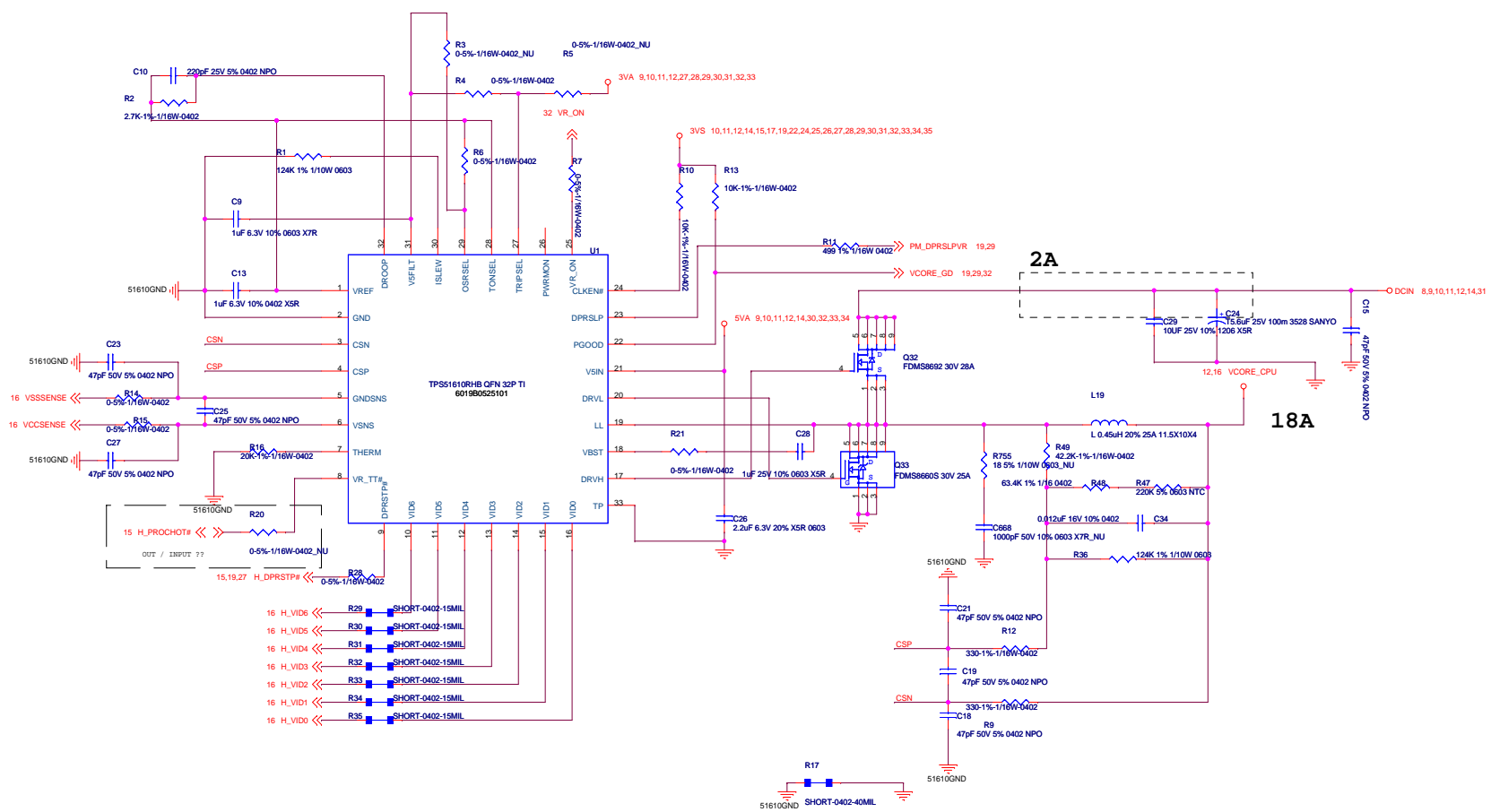


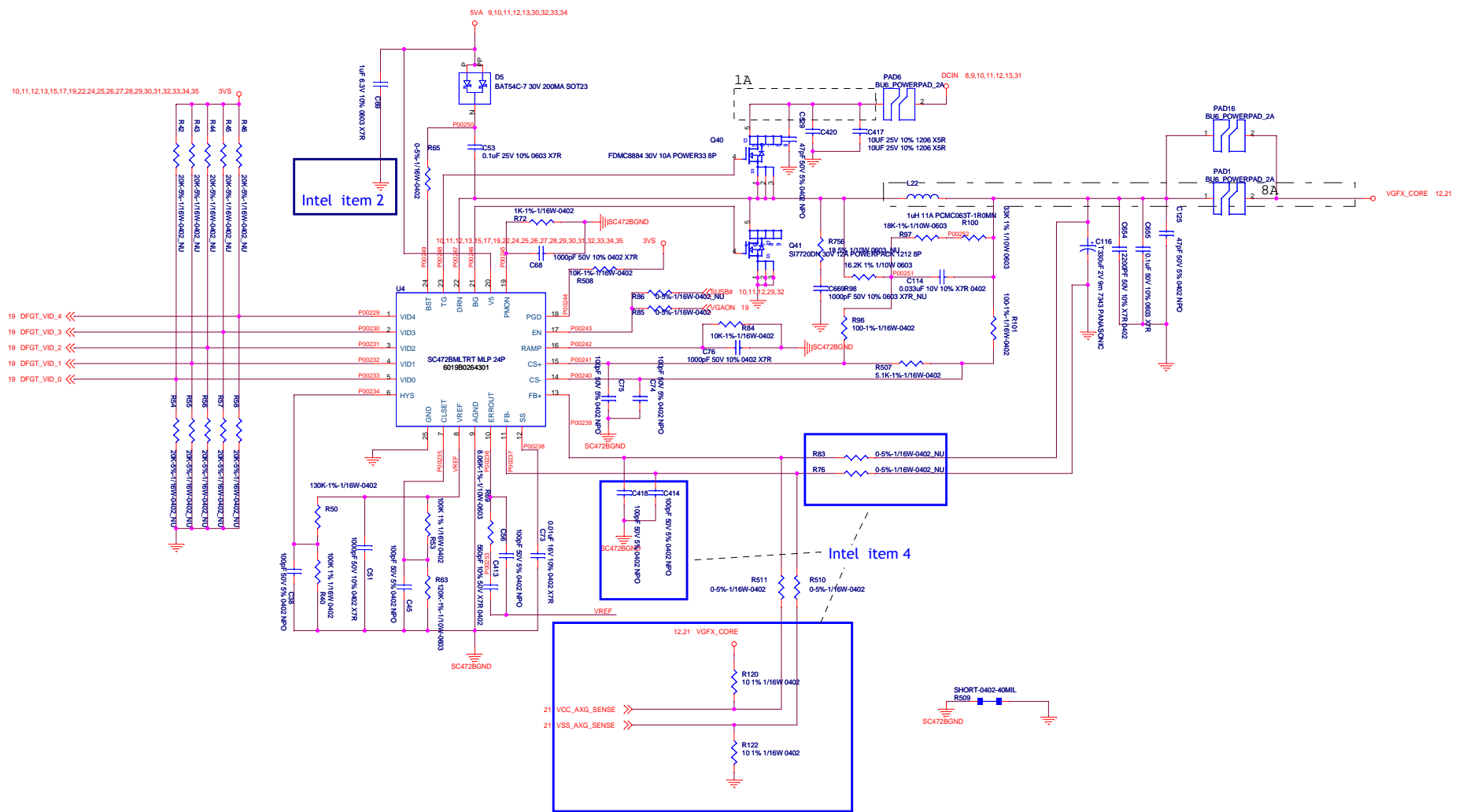
EMI Cap



For Green PC
None Green PC ---- NU





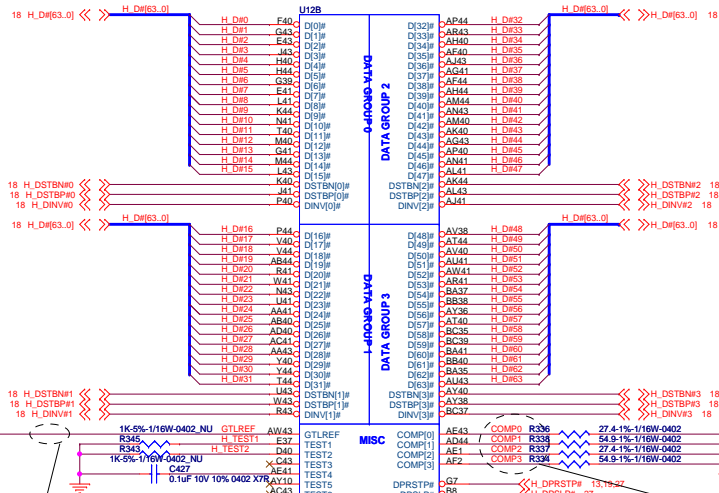
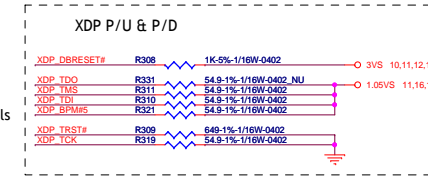


No stub on H_STPCLK test point

Route to TP via and place gnd via w/in 100mils

Should be connect to ICH9 and Cantiga without T-ing(no stub)

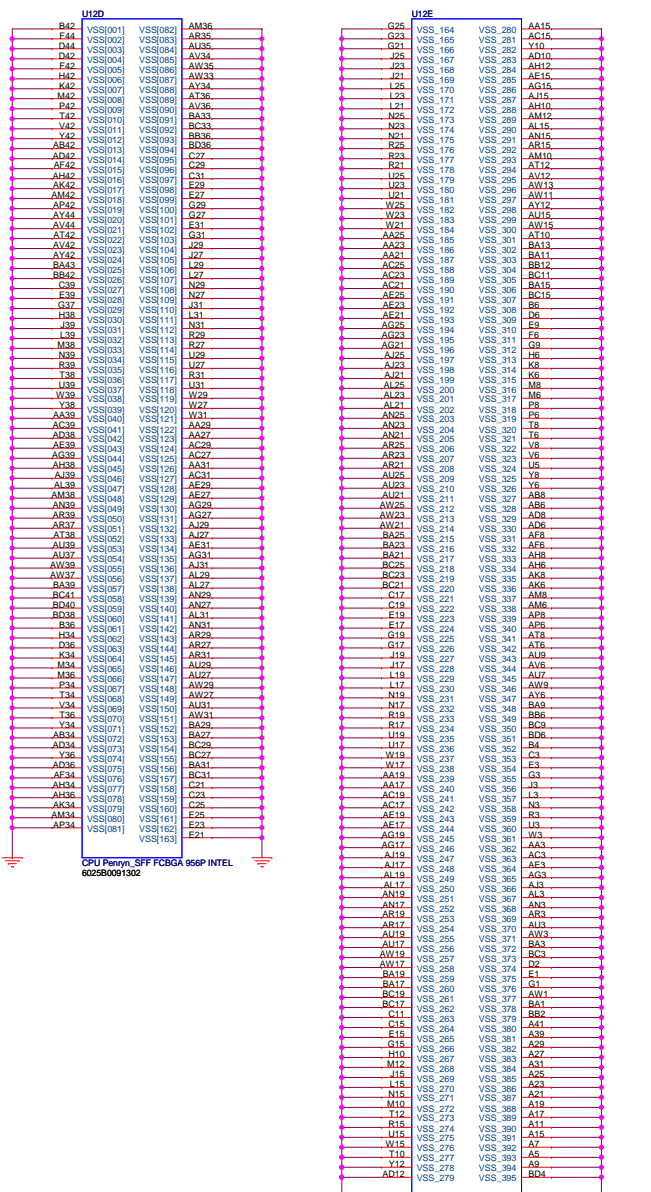
A#[32-39], APM#[0-1]:Leave escape routing on for future functionality



Zo=55ohm, 0.5" max for GTLREF, Space any other switch signals away from GTLREF with a minimum of 25mils. Don't allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals

H_PWRGD rise time : Max : 15ns

Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5" and width is 18mils. Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5" and width is 5mils



CPU PErmy SFF FCBSGA 556P INTEL 6025B0091302

12.13 VCORE_CPU

Place these inside socket cavity on L8
(North side secondary)

Place these inside socket cavity on L8
(South side secondary)

Place these inside socket cavity on L1
(North side Primary)

Place these inside socket cavity on L1
(South side Primary)

North side secondary

South side secondary

1.05VS_CPU 12

160mil

Place these inside socket cavity on L8
(North side secondary)

Close to CPU
pin B26

Impedance 55 Ohm, W:S= 1:2

Mismatch 25mil

18mil
7mil space
25mil space with other

Route VCCSENSE and VSSSENSE traces
at 27.4 ohms. Place PU and PD within
2 inch of CPU

CPU Penryn_SFF FCBGA 956P INTEL
6025B0091302

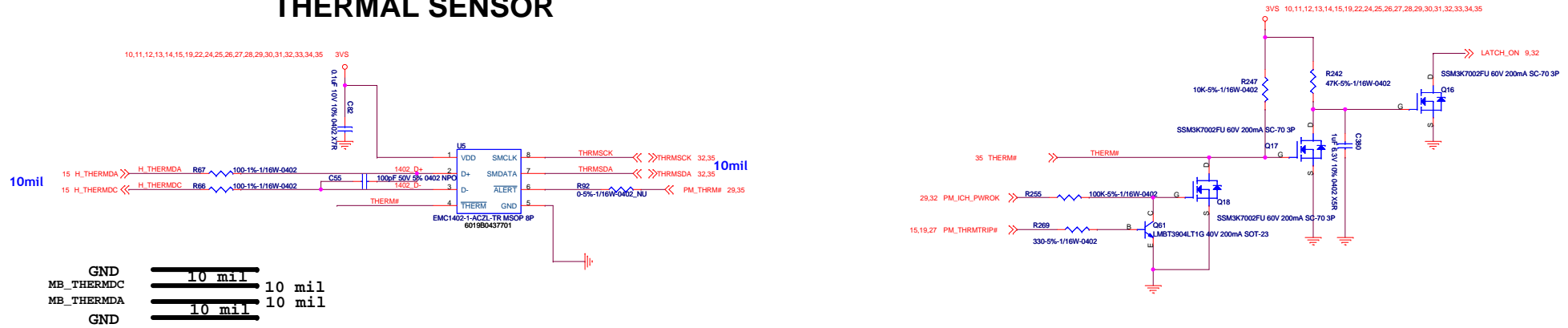
CPU Penryn_SFF FCBGA 956P INTEL
6025B0091302

INVENTEC
BAP31U
Penryn Processor(2/2)

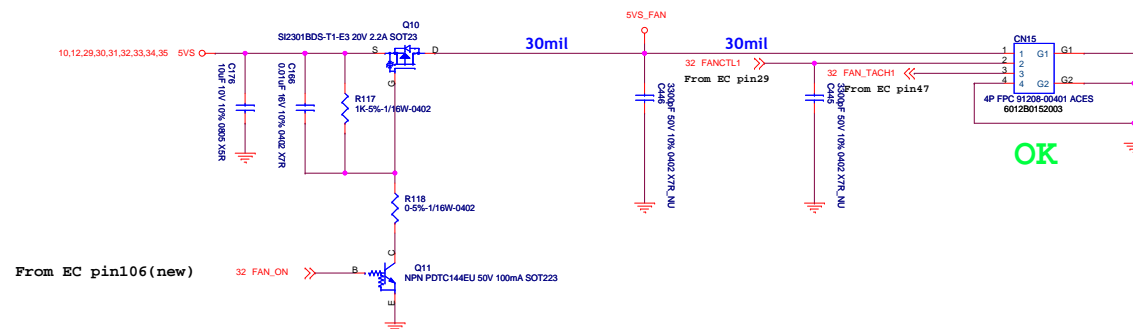
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Custom	AX1	D-CS-1310A2284501-ALG	A01
SHEET		16	25

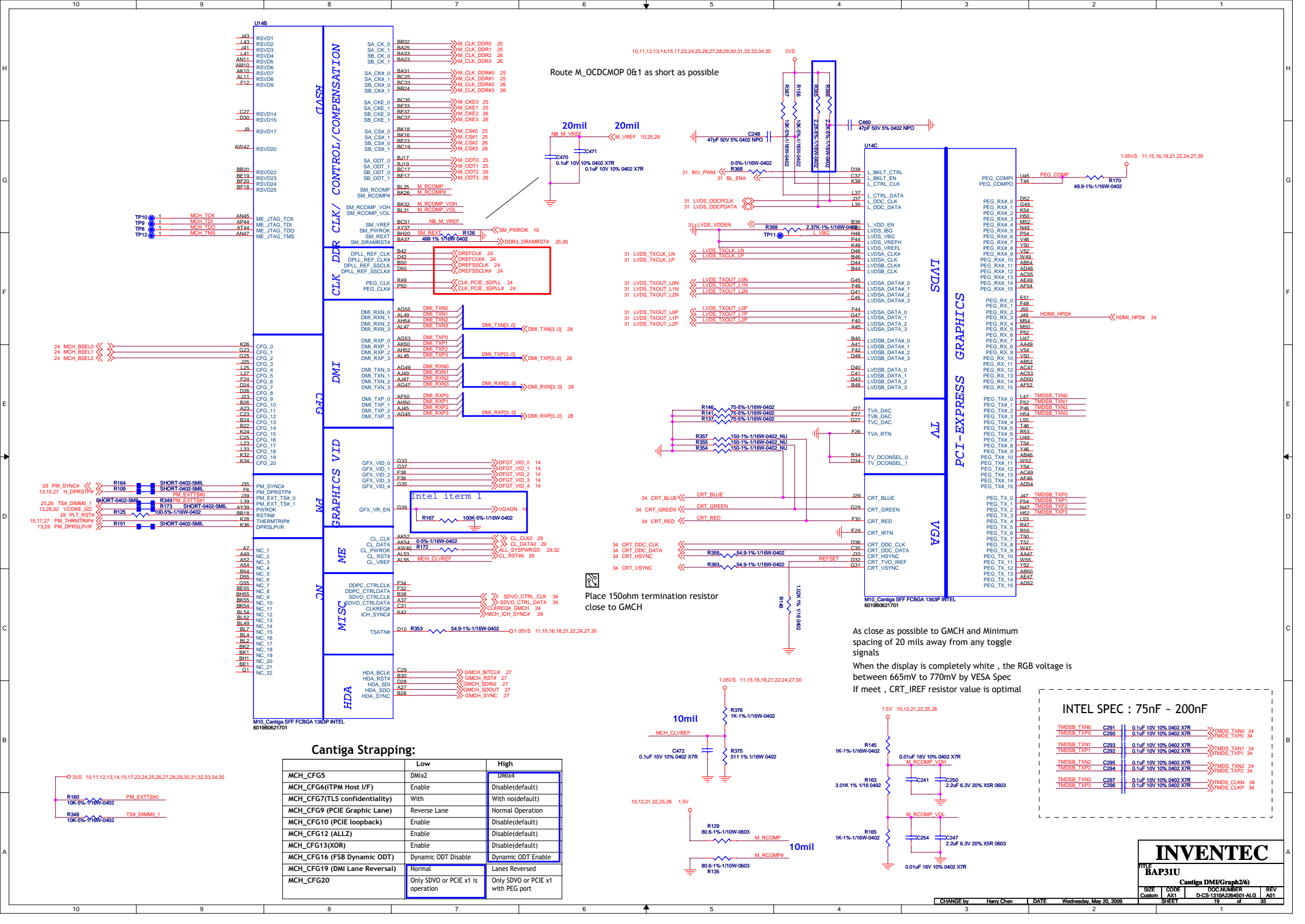
CHANGE by Harry Chen DATE Wednesday, May 20, 2009

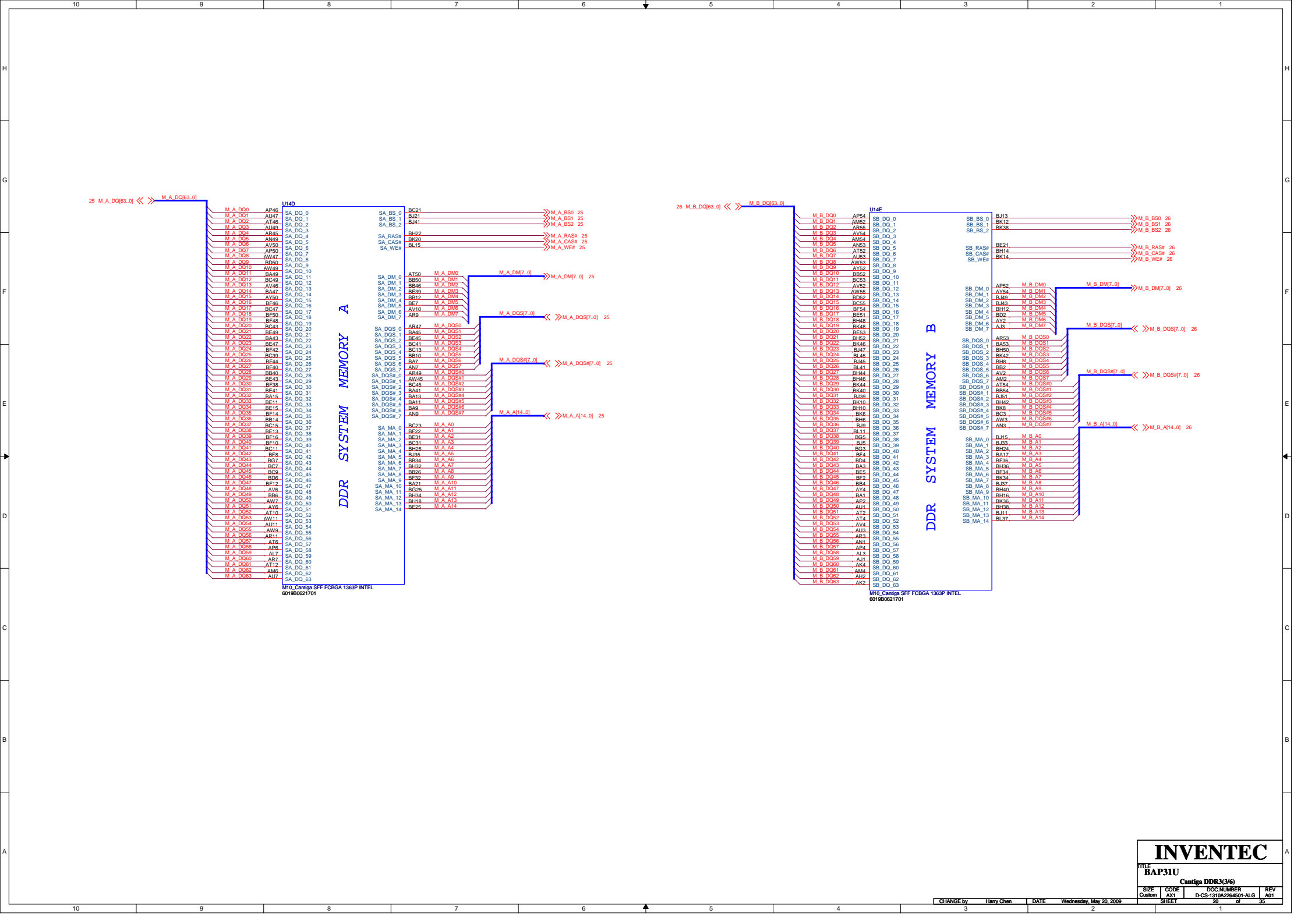
THERMAL SENSOR

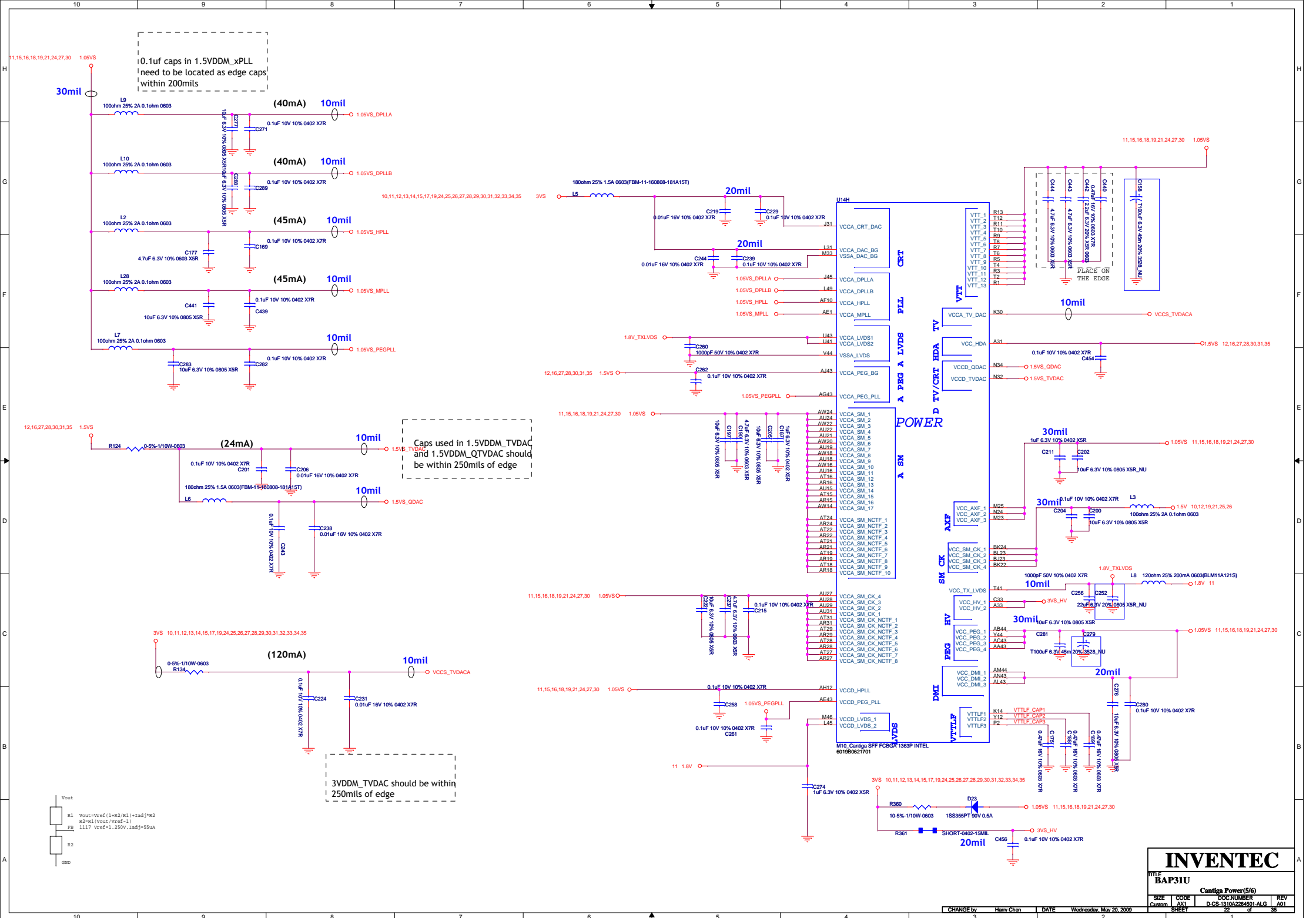


Fan control





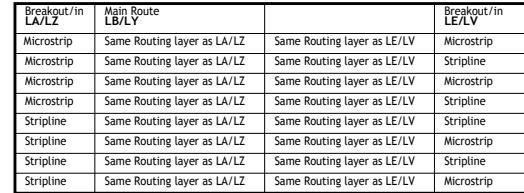


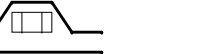


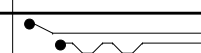

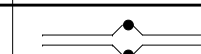
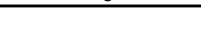
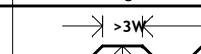

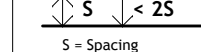


```

graph LR
    subgraph SMCH
        Tx[Tx]
        Rx[Rx]
    end
    subgraph ICH8m
        Rx2[Rx]
        Tx2[Tx]
    end
    Tx --> LA1[LA1]
    LA1 --> LA2[LA2]
    LA2 --> LB[LB]
    LB --> LC[LC]
    LC --> LD[LD]
    LD --> LE[LE]
    LE --> Rx2
    Rx2 --> LZ1[LZ1]
    LZ1 --> LZ2[LZ2]
    LZ2 --> LY[LY]
    LY --> LX[LX]
    LX --> LW[LW]
    LW --> LV[LV]
    LV --> Tx2

```

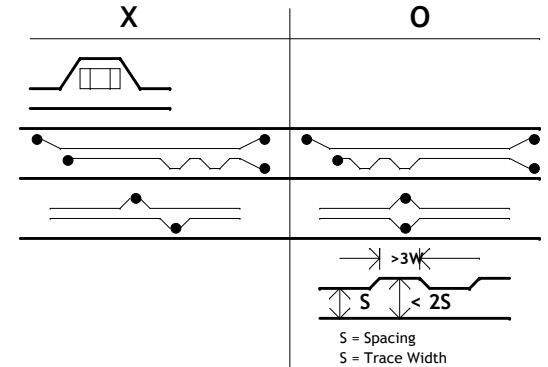


X	O
	
	
	
	
	 <p> $S = \text{Spacing}$ $S = \text{Trace Width}$ </p>

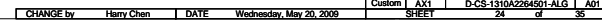
```

graph LR
    subgraph GMCH
        Tx1[Tx]
        Rx1[Rx]
        LA[LA]
        LB[LB]
        LZ[LZ]
        LY[LY]
    end
    subgraph ExpressMiniCard [Express/Mini Card]
        Rx2[Rx]
        Tx2[Tx]
    end
    Tx1 --- LA
    LA --- LB
    Rx1 --- LZ
    LZ --- LY
    LB --- Break(( ))
    Break --- LC[LC]
    LY --- LC
    LC --- Rx2
    LC --- Tx2

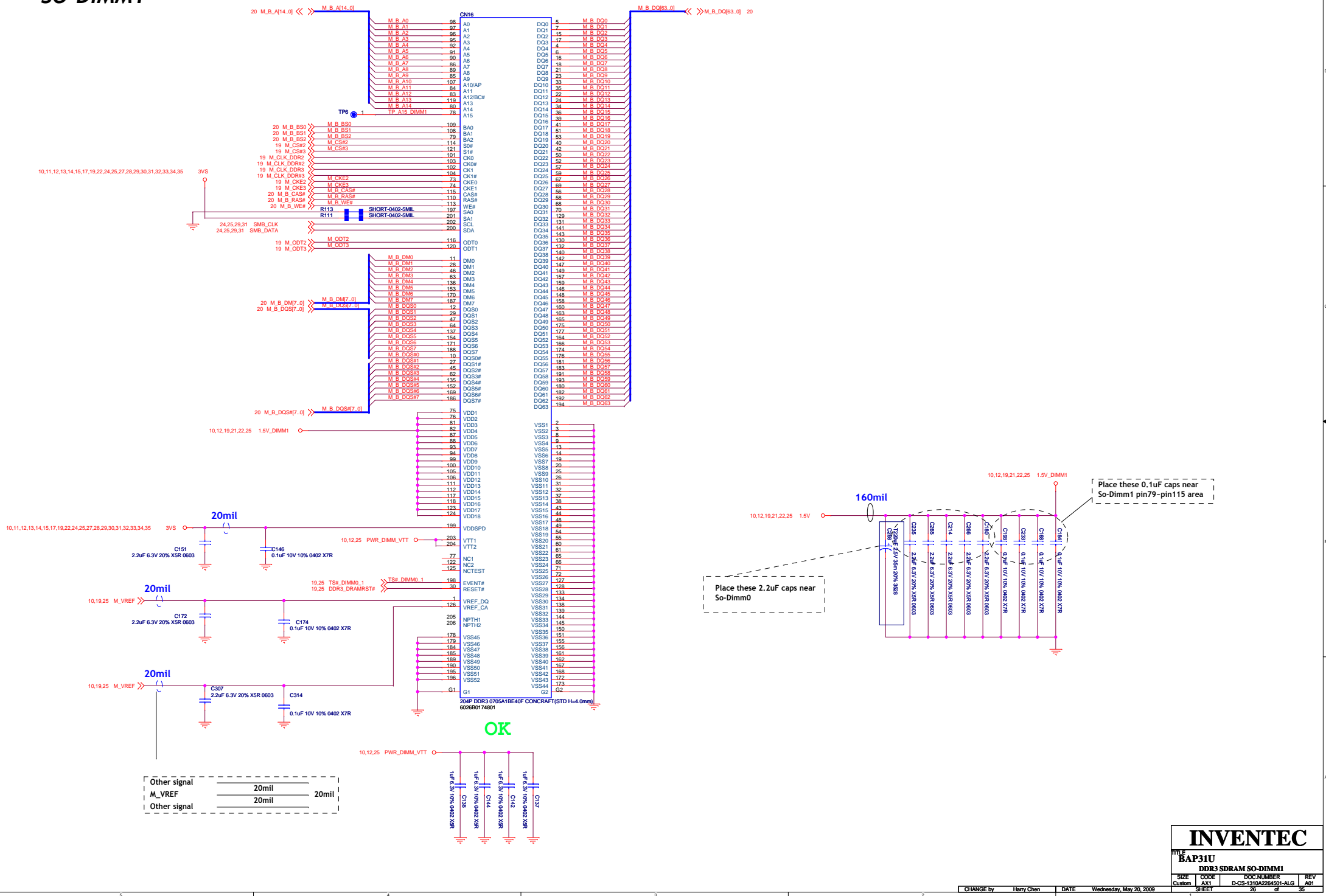
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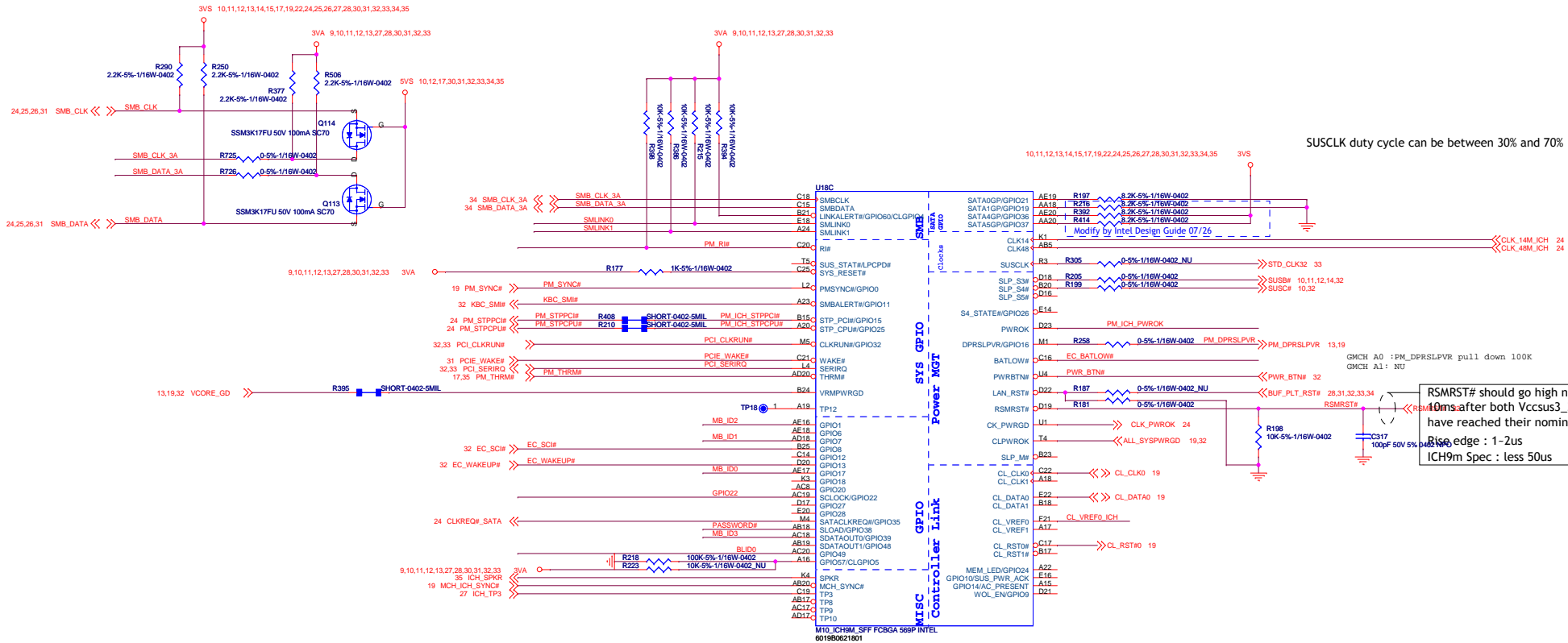


TITLE			
BAP31U			
Cantiga Ground(6/6)			
SIZE	CODE	DOC NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01
SHEET		23	of 35

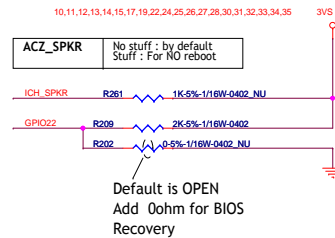


SO-DIMM1

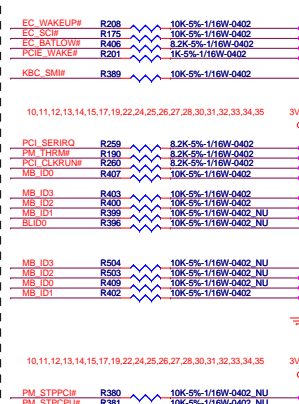




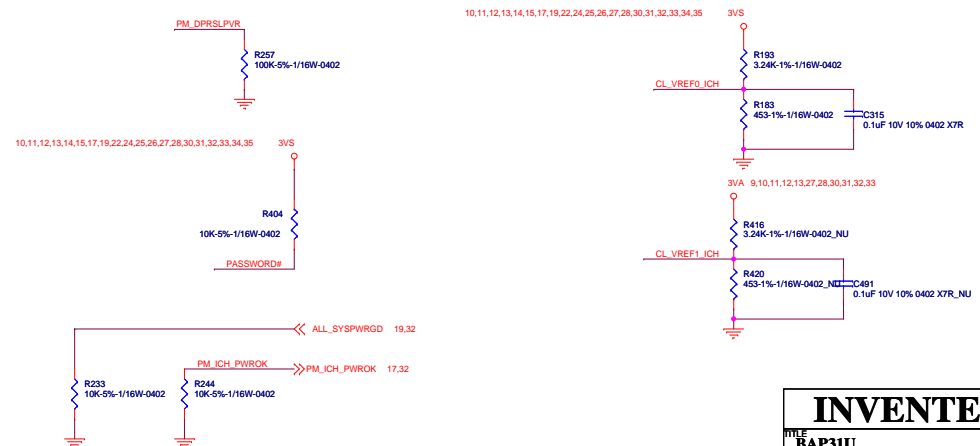
ICH9m strap



PMU P/U

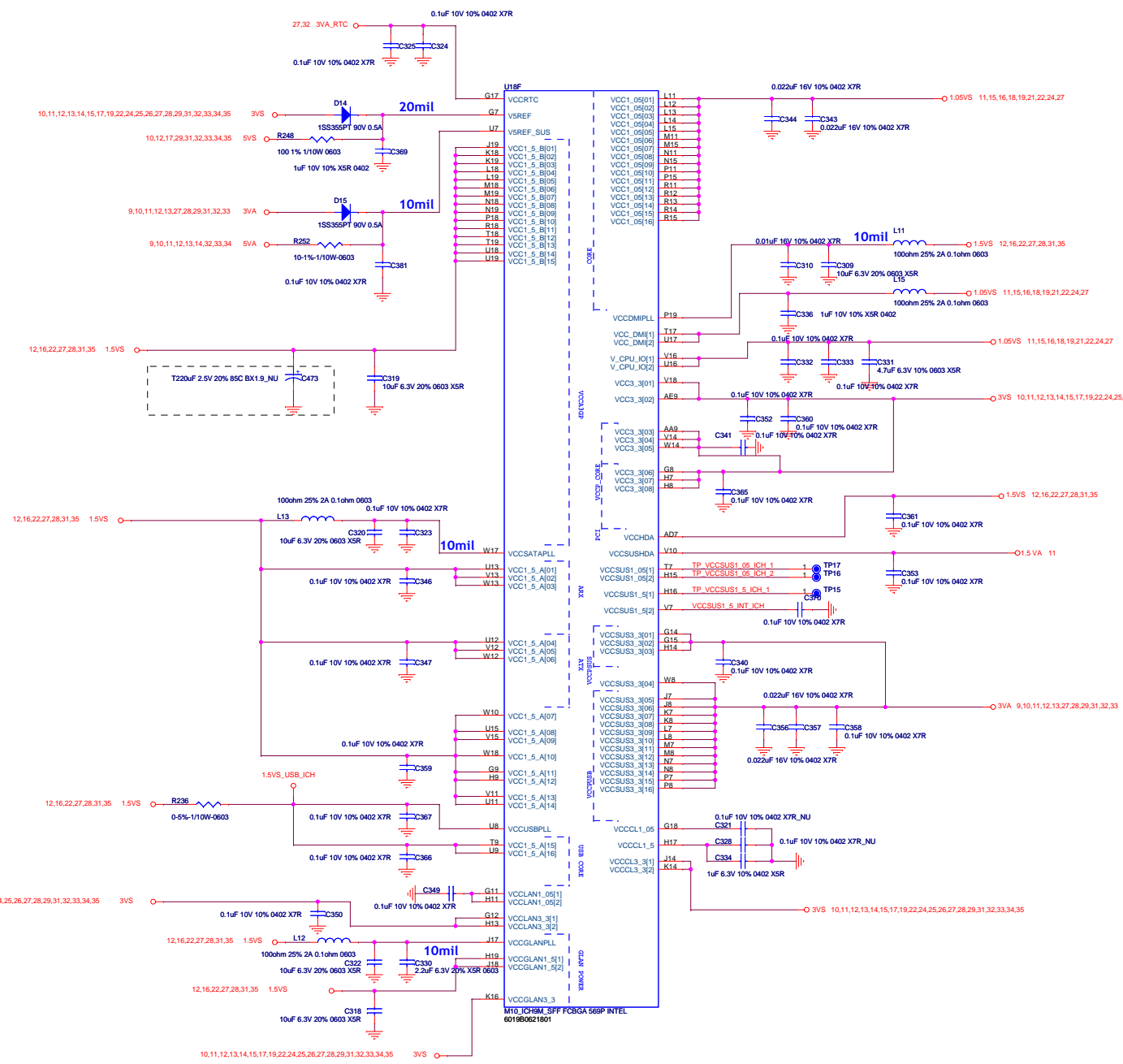


BIOS ID setting				
Project	MB_ID3	MB_ID2	MB_ID1	MB_ID0
JM31 (UMA)	1	1	1	1
SJM31 (UMA)	1	1	1	0
BAP31 (UMA)	1	1	0	1
	1	1	0	0
	1	0	1	1
	1	0	1	0
	1	0	0	1
	1	0	0	0
	0	1	1	1
	0	1	1	0
	0	1	0	1
	0	1	0	0
	0	0	1	1
	0	0	1	0
	0	0	0	1
	0	0	0	0



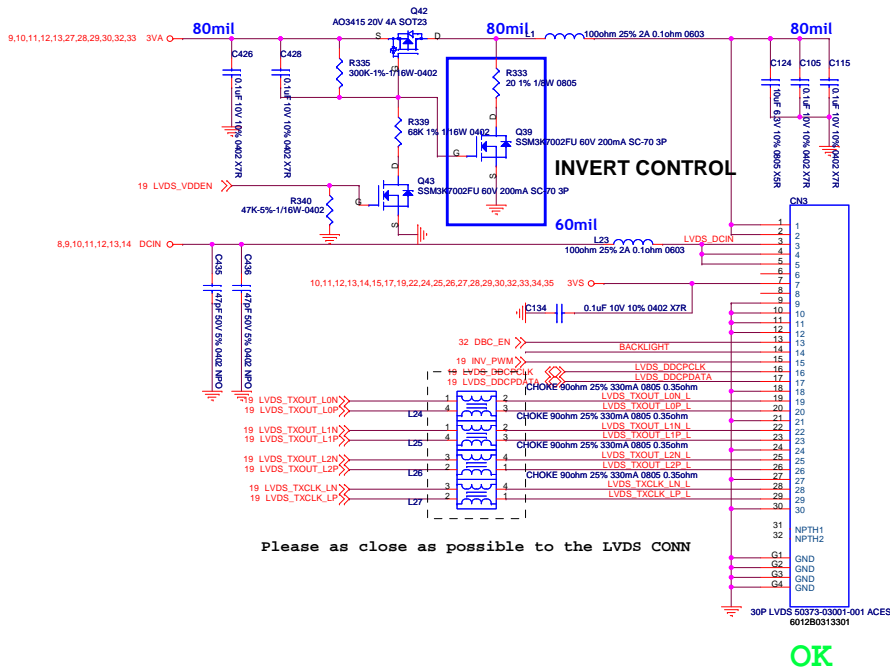
INVENTEC

FILE BAP31U ICH9M GPIO(3/4)			
SIZE	CODE	DOC NUMBER	REV
Custom	AX1	D-CS-1310A284501-ALG	A01
SHEET		29	35

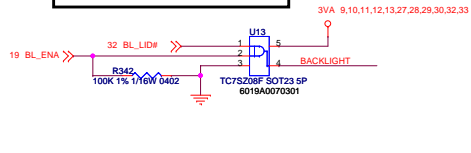


U1B	VSS[001]	VSS[107]	U6
B4	VSS[002]	VSS[108]	U10
B7	VSS[003]	VSS[109]	U11
B10	VSS[004]	VSS[110]	U14
B16	VSS[011]	VSS[116]	U16
B19	VSS[006]	VSS[112]	U21
B22	VSS[007]	VSS[113]	U25
D2	VSS[008]	VSS[114]	U5
D24	VSS[015]	VSS[115]	V3
E4	VSS[010]	VSS[116]	V19
E7	VSS[011]	VSS[117]	V23
E8	VSS[012]	VSS[118]	V24
E11	VSS[013]	VSS[119]	W4
E13	VSS[014]	VSS[120]	W11
E17	VSS[015]	VSS[121]	W7
E19	VSS[016]	VSS[122]	W9
E21	VSS[017]	VSS[123]	W15
F24	VSS[018]	VSS[124]	W19
G2	VSS[019]	VSS[125]	W21
G5	VSS[020]	VSS[126]	W22
G10	VSS[021]	VSS[127]	W25
G13	VSS[022]	VSS[128]	Y3
G16	VSS[023]	VSS[129]	Y23
G19	VSS[024]	VSS[130]	AA1
G21	VSS[025]	VSS[131]	AA4
H10	VSS[026]	VSS[132]	AA6
H12	VSS[027]	VSS[133]	AA8
H23	VSS[028]	VSS[134]	AA11
J5	VSS[029]	VSS[135]	AA13
J6	VSS[030]	VSS[136]	AA15
J10	VSS[031]	VSS[137]	AA17
J11	VSS[032]	VSS[138]	AA19
J12	VSS[033]	VSS[139]	AA21
J13	VSS[034]	VSS[140]	AA22
J21	VSS[035]	VSS[141]	AB3
J22	VSS[036]	VSS[142]	AB9
K2	VSS[037]	VSS[143]	AB13
K8	VSS[038]	VSS[144]	AB15
K10	VSS[039]	VSS[145]	AC1
K11	VSS[040]	VSS[146]	AC10
K12	VSS[041]	VSS[147]	AC12
K13	VSS[042]	VSS[148]	AC14
K15	VSS[043]	VSS[149]	AD2
K23	VSS[044]	VSS[150]	AD6
L5	VSS[045]	VSS[151]	AD16
L8	VSS[046]	VSS[152]	AD22
L10	VSS[047]	VSS[153]	AE1
L16	VSS[048]	VSS[154]	AE11
L21	VSS[049]	VSS[155]	AE13
L22	VSS[050]	VSS[156]	AE15
L25	VSS[051]	VSS[157]	AE17
M8	VSS[052]	VSS[158]	AE19
M10	VSS[053]	VSS[159]	AE25
M12	VSS[054]	VSS[160]	V9
M13	VSS[055]	VSS[161]	V17
M14	VSS[056]	VSS[162]	V19
M16	VSS[057]	VSS[163]	V23
M17	VSS[058]	VSS[164]	V25
M23	VSS[059]	VSS[165]	W1
N2	VSS[060]	VSS[166]	W11
N5	VSS[061]	VSS[167]	W15
N8	VSS[062]	VSS[168]	W19
N10	VSS[063]	VSS[169]	W21
N12	VSS[064]	VSS[170]	W23
N13	VSS[065]	VSS[171]	W25
N14	VSS[066]	VSS[172]	Y3
N17	VSS[067]	VSS[173]	Y23
N21	VSS[068]	VSS[174]	AA1
N22	VSS[069]	VSS[175]	AA4
N25	VSS[070]	VSS[176]	AA6
P10	VSS[071]	VSS[177]	AA8
P12	VSS[072]	VSS[178]	AA11
P13	VSS[073]	VSS[179]	AA13
P16	VSS[074]	VSS[180]	AA15
P17	VSS[075]	VSS[181]	AA17
P22	VSS[076]	VSS[182]	AA19
P23	VSS[077]	VSS[183]	AA21
P24	VSS[078]	VSS[184]	AA22
P25	VSS[079]	VSS[185]	AB3
P26	VSS[080]	VSS[186]	AB9
P27	VSS[081]	VSS[187]	AB13
P28	VSS[082]	VSS[188]	AB15
P29	VSS[083]	VSS[189]	AC1
P30	VSS[084]	VSS[190]	AC10
P31	VSS[085]	VSS[191]	AC12
P32	VSS[086]	VSS[192]	AC14
P33	VSS[087]	VSS[193]	AD2
P34	VSS[088]	VSS[194]	AD6
P35	VSS[089]	VSS[195]	AD16
P36	VSS[090]	VSS[196]	AD22
P37	VSS[091]	VSS[197]	AE1
P38	VSS[092]	VSS[198]	AE11
P39	VSS[093]	VSS[199]	AE13
P40	VSS[094]	VSS[200]	AE15
P41	VSS[095]	VSS[201]	AE17
P42	VSS[096]	VSS[202]	AE19
P43	VSS[097]	VSS[203]	AE25
P44	VSS[098]	VSS[204]	V9
P45	VSS[099]	VSS[205]	V17
P46	VSS[100]	VSS[206]	V19
P47	VSS[101]	VSS[207]	V23
P48	VSS[102]	VSS[208]	V25
P49	VSS[103]	VSS[209]	Y3
P50	VSS[104]	VSS[210]	Y23
P51	VSS[105]	VSS[211]	AA1
P52	VSS[106]	VSS[212]	AA4

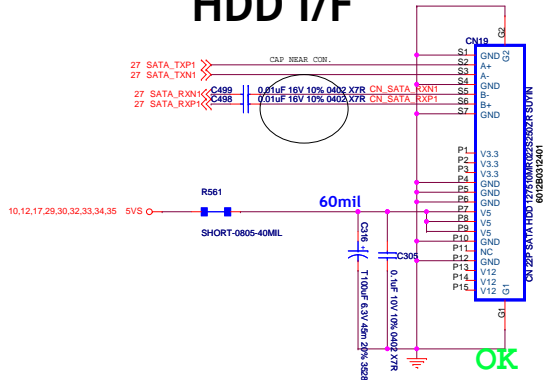
LVDS Interface



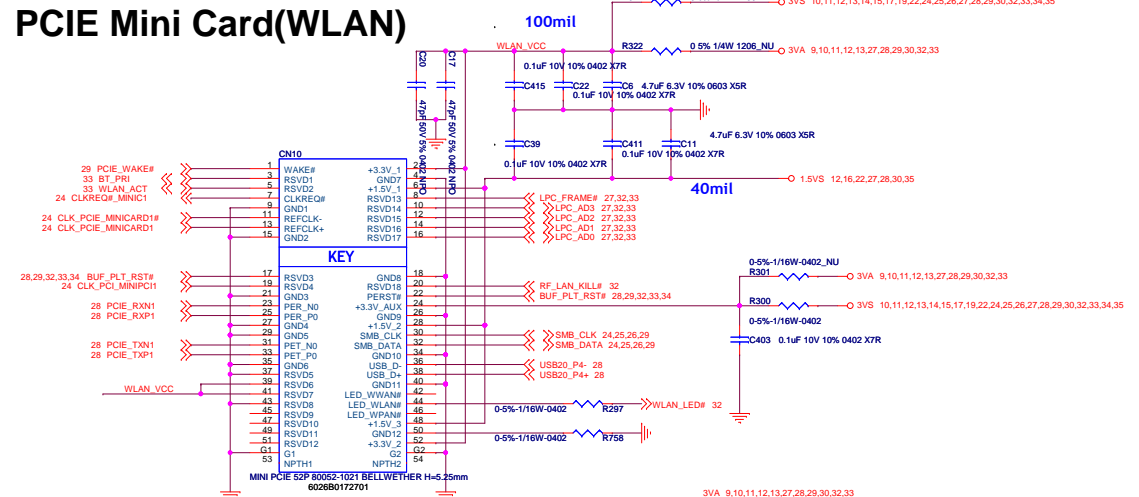
LCD brightness control



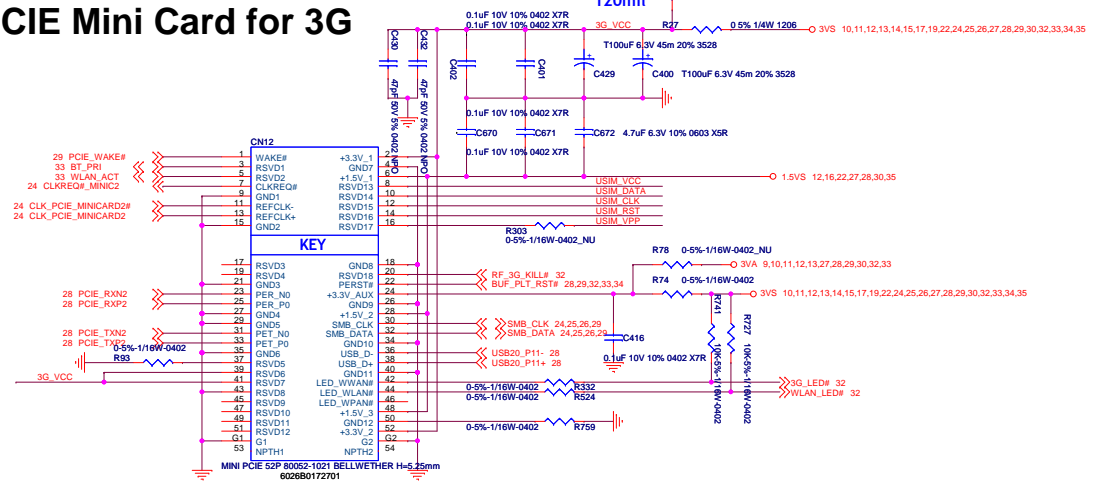
HDD I/F



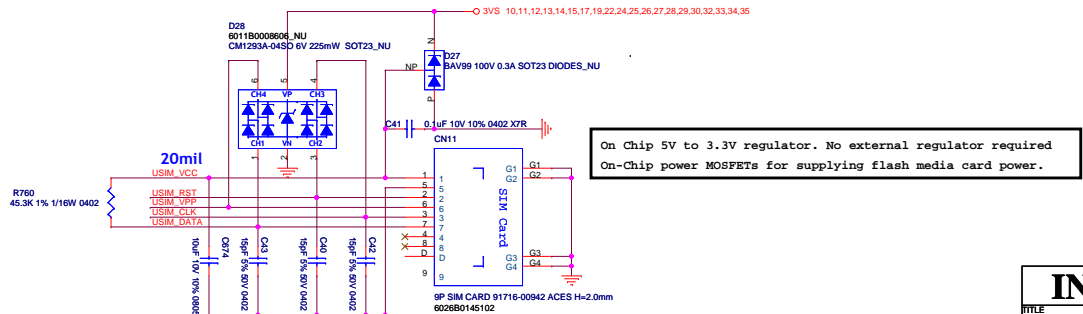
PCIE Mini Card(WLAN)



PCIE Mini Card for 3G



SIM CARD slot



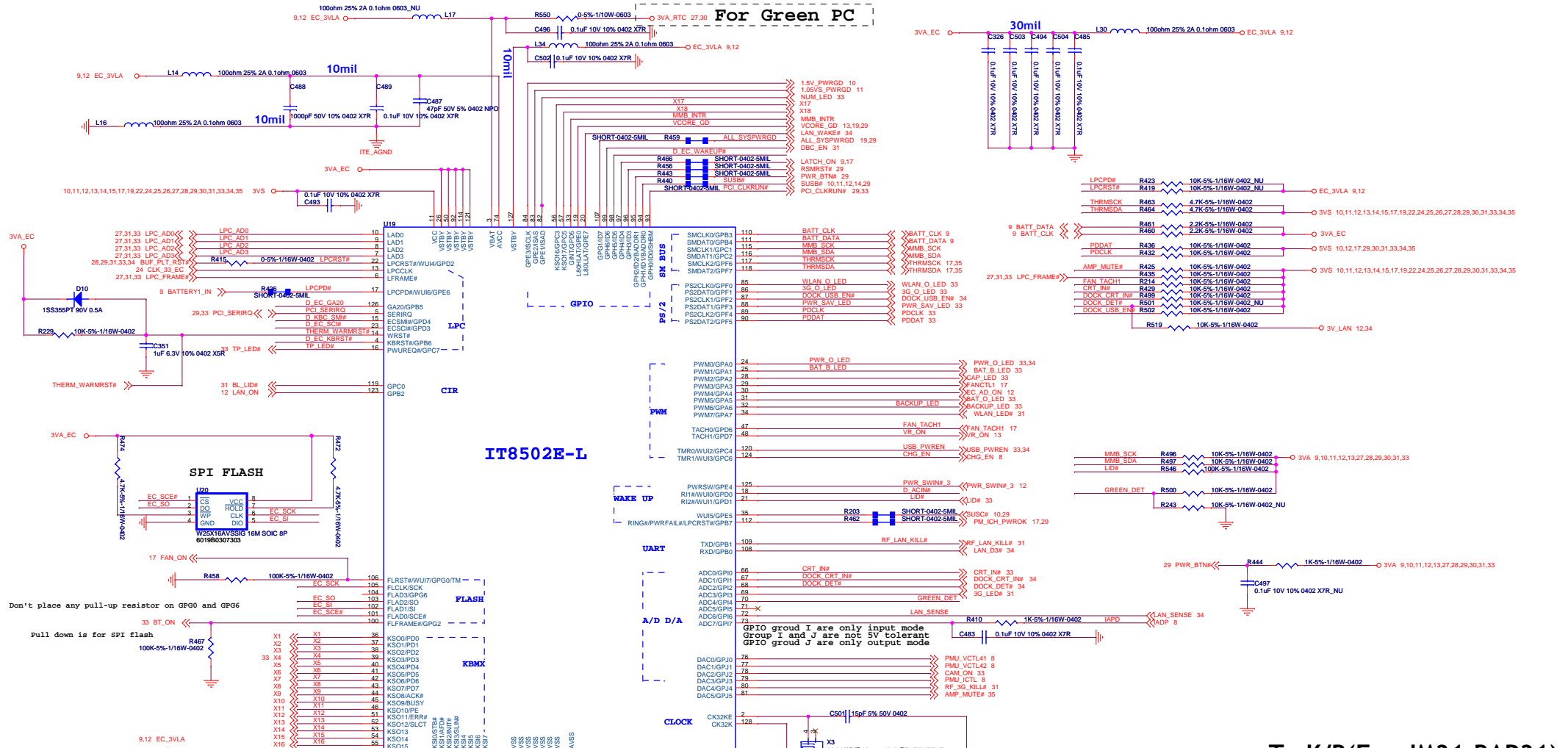
OK, 12/26

INVENTEC

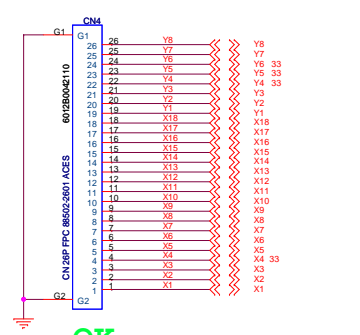
TITLE BAP31U			
LCD CNN & WLAN & 3G			
SIZE	CODE	DOC NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01
SHEET		31 of 36	

CHANGE by Harry Chen DATE Wednesday, May 20, 2009

For Green PC



To K/B(For JM31,BAP31)



INVENTEC			
TITLE: BAP31U			
KBC ITERS12F/IO			
SIZE	CODE	DOC NUMBER	REV
Custom	AX1	D-CS-1310A2264501-ALG	A01
SHEET 32 of 35			

